

WHAT IS CLAIMED is:

1. A semiconductor device comprising:

a semiconductor substrate;

5 a gate electrode provided on a gate insulating
film formed on the surface of the semiconductor
substrate;

a post-oxide film comprising a first portion,
a second portion and a third portion, the first portion
extending on a sidewall of the gate electrode to the
10 surface of the semiconductor substrate, the second
portion extending on the surface of the semiconductor
substrate and contacting with the first portion,
the third portion extending on the surface of the
semiconductor substrate with its end contacting with
15 an end of the second portion opposite to the first
portion and thinner than the second portion;

a spacer covering a sidewall of the first portion
on the second portion and the third portion;

20 source/drain extension layers formed in the
surface of the semiconductor substrate under the second
portion and/or third portion and sandwiching a channel
region under the gate electrode; and

25 source/drain diffusion layers formed in the
surface of the semiconductor substrate and contacting
with ends of the source/drain diffusion opposite from
the channel region.

2. The semiconductor device according to claim 1,

wherein

the semiconductor device includes an array transistor that forms a part of a memory cell and a peripheral transistor that forms a part of
5 a peripheral circuit, and

the array transistor and the peripheral transistor have the gate electrode, the post-oxide film, the spacer, the source/drain extension layers, and the source/drain diffusion layers.

10 3. The semiconductor device according to claim 1, wherein the width of the spacer is no greater than 30 nm.

4. The semiconductor device according to claim 3, wherein the length of the second portion from its one
15 end contacting with the first portion to its other end contacting with the third portion is no greater than 30 nm.

5. The semiconductor device according to claim 4, wherein the second portion is thicker than the first
20 portion.

6. The semiconductor device according to claim 1, wherein the thickness of the second portion is no less than 10 nm.

7. The semiconductor device according to claim 6,
25 wherein the thickness of the third portion is no greater than 10 nm.

8. A method of manufacturing a semiconductor

device having an array transistor that forms a part of
a memory cell formed in an array transistor area and
a peripheral transistor that forms a part of
a peripheral circuit formed in a peripheral area,
5 comprising:

forming a gate electrode on a gate insulating film
on the surface of a semiconductor substrate in the
array transistor area and the peripheral area;

10 forming a first post-oxide film on the sidewall of
the gate electrode in the array transistor area and the
peripheral area;

forming first source/drain extension layers in the
surface of the semiconductor substrate in the array
transistor area, the first source/drain extension
15 layers sandwiching a channel region below the gate
electrode;

forming a second post-oxide film on the surface of
the semiconductor substrate in the vicinity of the gate
electrode so that it comes into contact with the first
20 post-oxide film;

forming second source/drain extension layers in
the surface of the semiconductor substrate in the
peripheral area by ion implantation through the second
post-oxide film and a third post-oxide film formed on
25 the semiconductor substrate, the third post-oxide film
contacting with ends of the second post-oxide film
opposite from the first post-oxide film; and

forming source/drain diffusion layers in the surface of the semiconductor substrate in the array transistor area and the peripheral area, the source/drain diffusion layers contacting with ends of the first and second source/drain extension layers opposite from the channel region.

9. The method according to claim 8, wherein forming the second post-oxide film includes

forming an oxide film comprising a first portion on the sidewall of the gate electrode which forms the first post-oxide film and a second portion located on the surface of the semiconductor substrate,

forming a insulating film on the second portion to cover the sidewall of the first portion, and

removing the second portion which is not covered by the insulating film.

10. The method according to claim 9, wherein forming the first source/drain extension layers includes performing ion implantation through the second portion of the oxide film before the insulating film is removed.

11. The method according to claim 8, wherein the second post-oxide film is a layer of native oxide formed together with the third post-oxide film.

12. The method according to claim 11, further comprising before the second post-oxide film is formed forming an oxide film comprising a first portion

on the sidewall of the gate electrode which forms the first post-oxide film and a second portion located on the surface of the semiconductor substrate and removing the second portion.